TSMC-03-065

January 5, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
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Subject: Serial No. 10/688,045 10/17/03

Huan-Just Lin et al.

FULLY DRY, Si RECESS FREE PROCESS FOR REMOVING HIGH K DIELECTRIC LAYER

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 27, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 1/27/04

U.S. Patent 6,258,675 to Gardner et al., "High K Gate Electrode," discusses a silicon nitride interfacial layer used both above and below a high K dielectric layer.

U.S. Patent 6,306,715 to Chan et al., "Method to Form Smaller Channel with CMOS Device by Isotropic Etching of the Gate Materials," describes a method for isotropically etching a metal oxide such as HfO2.

U.S. Patent 6,492,242 to See et al., "Method of Forming of High K Metallic Dielectric Layer," discusses a high k dielectric layer which is Ta2O5, CuO2, Al2O3 or TiO2 formed as part of a metal-oxide-metal capacitor.

U.S. Patent 6,479,403 to Tsei et al., "Method to Pattern Polysilicon Gates with High-K Material Gate Dielectric," discusses a high k dielectric layer deposited on a partially formed transistor structure and is preferably etched with an argon sputter method.

U.S. Patent 6,451,647 to Yang et al., "Integrated Plasma Etch of Gate and Gate Dielectric and Low Power Plasma Post Gate Etch Removal of High-K Residual," describes a method for removing a high k dielectric layer and includes a plasma etch comprised of a fluorocarbon, O2, and an inert gas.

U.S. Patent 6,436,838 to Ying et al., "Method of Patterning Lead Zirconium Titanate and Barium Strontium Titanate," discusses an etch chemistry comprised of BCl3, an inert gas, and optionally O2, N2, or Cl2 is used to selectively etch a ferroelectric layer such as PZT or BST in the presence of SiO2.

TSMC-01-1248, Serial No. 10/653,852, filed 09/03/03, assigned to a common assignee, "Method of Multi-element Compound Deposition by Atomic Layer Deposition for IC Barrier Layer Applications," discloses an atomic layer deposition (ALD) method of forming a multi-element film that is used as a diffusion barrier layer or as a gate dielectric layer during the fabrication of a semiconductor device.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-03-065	10/688,045
Applicant: Huan-Just Lin et al.	
Filing Date: 10/17/03	Group Art Unit:

OIPE JC26 JAN 29 2004 PATENT & TRADEMARK OFFICE

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6258675	7/10/01	Gardner et al.	438	287	12/18/97
	6306715	10/23/01	Chan et al.	438	301	1/8/01
	6492242	12/10/02	See et al.	438	393	7/3/00
	6479403	11/12/02	Tsei et al.	438	778	2/28/02
	6451647	9/17/02	Yang et al.	438	240	3/18/02
	6436838	8/20/02	Ying et al.	438	710	4/21/00

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	TSMC-01-1248, Ser. No. 10/653,852, Filed 09/03/03, assigned to a common assignee, "Method of Muti-element Compound Deposition by Atomic Layer Deposition for IC Barrier Layer Applications".

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.